

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

5 Listing of Claims:

Claim 1 (Currently Amended): A counter comprising:
a plurality of state units for generating a state, each
state unit having a corresponding clock end for receiving
10 a clock having a plurality of pulses; wherein each said
state unit is capable of updating the its corresponding
state when receiving different pulses from the clock
according to a predetermined law while each ~~of the state~~
units said state unit receives the clock from the its
15 corresponding clock end; and
a clock gating circuit electrically connected to the
plurality of state units for selecting at least one first
state unit and at least one second state unit from the
plurality of state units according only to a ~~fixed an~~
20 initial value and providing a triggering clock to the
clock end of each said at least one first state unit and
withholding the triggering clock from the clock end of
each said at least one second state unit, such that second
states corresponding to each said at least one second
25 state unit are held constant while each ~~of the said at~~
least one first state units unit updates each its state
corresponding to ~~the first state units said at least one~~
first state unit according to different pulses of the
triggering clock; wherein the clock gating circuit net
30 providing does not provide the triggering clock to each
~~of the second state units said at least one second state~~
unit according to each state changed of the said at least

one first state unit, and ~~not withholding~~ does not withhold the triggering clock from each said at least one first state unit of the first state units; and a latch circuit connected to the clock gating circuit for 5 storing the initial value.

Claim 2 (Currently Amended): The counter of claim 1 wherein the clock gating circuit selects corresponding different said at least one first state units unit and said at least one second state units unit from the plurality of state units while the initial value changes.
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Claim 3 (Currently Amended): The counter of claim 1 wherein each ~~of the state units~~ said state unit further comprises a setting end for receiving an initial state so that the each said state unit outputs the initial state while the each said state unit is first triggered by a clock pulse received from the corresponding clock end, then updates 15 its corresponding state output when receiving a following pulse of the clock according to the predetermined law.
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Claim 4 (Currently Amended): The counter of claim 3 wherein the counter is capable of setting each the initial state of the each said state unit from each the setting end of the each said state unit according to the initial value while the clock gating circuit selects the said at least one first state unit and the said at least one second state unit according to the initial value.
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Claim 5 (Cancelled)

Claim 6 (Currently Amended): The counter of claim 1 wherein each of the state units said state unit further comprises a flip-flop.

5 Claim 7 (Currently Amended): A method for a counter, the counter comprising:

a plurality of state units for generating a state, each state unit having a corresponding clock end for receiving a clock having a plurality of pulses; wherein each said state unit is capable of updating the its corresponding state when receiving different pulses from the clock according to a predetermined law while each of the state units said state unit receives the clock from the its corresponding clock end; and

15 a latch circuit connected to a clock gating circuit for storing an initial value;

the method comprising:

selecting at least one first state unit and at least one second state unit from the plurality of state units according only to a fixed the initial value and providing a triggering clock to the clock end of each said at least one first state unit and withholding the triggering clock from the clock end of each said at least one second state unit, such that second states corresponding to the each said at least one second state unit are held constant while each of the first state units said at least one first state unit updates each its state corresponding to the first state units said at least one first state unit according to different pulses of the triggering clock.

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Claim 8 (Cancelled)

- Claim 9 (Currently Amended): The method of claim 7 further comprising selecting different said at least one first state unit and said at least one second state unit from the plurality of state units while the initial value changes.
- 5 the at least one first state unit and the at least one second state unit according to the initial value for different initial values to select corresponding different first state units and second state units from the plurality of state units.
- 10 Claim 10 (Currently Amended): The method of claim 7 wherein each of the state units said state unit further comprises a setting end for receiving an initial state so that the each said state unit outputs the initial state while the each said state unit is first triggered by a clock pulse received from the corresponding clock end, then updates its corresponding state output when receiving a following pulse of the clock according to the predetermined law.
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- 20 Claim 11 (Currently Amended): The method of claim 10 further comprising setting each the initial state of the each said state unit from each the setting end of the each said state unit according to the initial value while selecting the said at least one first state unit and the said at least one second state unit according to the initial value.
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Claim 12 (Cancelled)

- 30 Claim 13 (Currently Amended): The method of claim 7 wherein each of the state units each said state unit further comprises a flip-flop.